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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,178	03/11/2004	Cheng-Ku Chen	TS03-375	5314

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EXAMINER	
LEE, CHEUNG	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,178	CHEN ET AL.	
	Examiner	Art Unit	
	Cheung Lee	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☒ Claim(s) *8 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/6/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on May 6, 2004 was filed before the first action on the merits. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

2. Claims 15-27 are objected to because of the following informalities: in claim 15, line 11-12, deletion of "silicon dioxide" is suggested for correctness.

Claims 16-27 depend from claim 16, so they are objected for the same reason.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3,5-7, 9-10, and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (US Pat 6350639; hereinafter "Yu").

4. With respect claim 1, referring to figures 3A-4F, Yu discloses a method of forming a metal oxide semiconductor field effect transistor (MOSFET) (col. 11, lines 6-13) on a semiconductor substrate 102, comprising the steps of: providing a gate

insulator layer 116, and an overlying conductive layer 114 on said semiconductor substrate; forming a mask shape 124, 126 on said conductive layer; performing a first etch procedure using said mask shape (col. 8, lines 62-67; fig. 3C) to form a tapered conductive gate structure on said gate insulator layer with top surface of said conductive gate structure comprised with a smaller width than a bottom surface of said tapered conductive gate structure 328, 330; performing an ion implantation procedure (col. 11, lines 15-34) to form a lightly doped source/drain (LDD) region in an area of said semiconductor substrate not covered by said tapered conductive gate structure (see figs. 4A and 4C), and to inherently implant ions into portions of said tapered conductive gate structure, through tapered sides of said tapered conductive gate structure (figs. 4A and 4C, items 432 and 440); performing a second etch procedure to remove portions of said tapered conductive gate structure comprised with said implanted ions (col. 11, lines 37-52) resulting in a straight walled conductive gate structure 358, 360, and resulting in said LDD region offset from edges of said straight walled conductive gate structure (fig. 4E); forming sidewall spacers on said straight walled conductive gate structure 148, 150; and forming a heavily doped source/drain region 458, 460, 466, and 468 in an area of said semiconductor substrate not covered by said straight walled conductive gate structure of by said sidewall spacers (col. 11, lines 53-67). Yu discloses anisotropic etching to form tapered and straight walled gate structures, but Yu does not disclose expressly dry etching. However, the examiner takes official notice that anisotropic etch is conventionally done by dry etching.

5. With respect to claim 2, Yu discloses said MOSFET device is an N channel (NMOS) device (col. 1, lines 19-28).

6. With respect to claim 3, Yu discloses said MOSFET device is a P channel (PMOS) device (col. 1, lines 19-28).

7. With respect to claims 5 and 7, Yu does not disclose expressly wherein [Claim 5] said mask shaped is comprised of silicon nitride; [Claim 7] said mask shaped is comprised of silicon oxide. However, Yu discloses the mask shape materials include various oxides and nitrides (col. 5, lines 1-11). The examiner takes the position that it is obvious to use silicon oxide and silicon nitride as the mask shape.

8. With respect to claim 6, Yu discloses said mask shape is comprised of silicon oxynitride (col. 5, lines 1-11).

9. With respect to claim 9, Yu does not disclose expressly wherein the width of the bottom of said tapered conductive gate structure is between about 100 to 200 Angstroms larger than the width of the top of said tapered conductive gate structure. However, Yu discloses the distance between LDD regions and the straight walled gate's edges can be adjusted by controlling the sloped profiles of the sidewalls 329 (col. 11, lines 37-52). So, the top and bottom widths of tapered gate are adjustable and controllable. Any variation in top and bottom widths of tapered gate in the present claim is obvious in light of the cited art, because the changes in top and bottom widths of tapered gate produce no unexpected function. The routine varying of parameters to produce expected changes are within the ability of one of ordinary skill in the part. Patentability over the prior art will only occur if the parameter variation produces an

unexpected result. *In re Aller, Lacey and Hall*, 105 USPQ 233, 235. *In re Reese* 129 USPQ 402, 406.

10. With respect to claims 10 and 14, Yu discloses wherein [Claim 10] said ion implantation procedure is performed using arsenic or phosphorous ions (col. 4, lines 41-55; col. 11, lines 15-34); [Claim 14] said heavily doped source/drain region is formed via implantation of arsenic or phosphorus ions (col. 4, lines 41-55; col. 11, lines 53-60), but Yu does not disclose expressly wherein ion implantation procedure is performed at an energy between about 3 to 10 KeV, at a dose about 1E12 to 1E14 atoms/cm^2 for LDD region, and at an energy between about 30 to 100 KeV, at a dose between about 1E15 to 1E16 atoms /cm^2 for heavily doped source/drain region. However, any variation in ion implantation energy and dose in the present claim is obvious in light of the cited art, because the changes in ion implantation energy and dose produce no unexpected function. The routine varying of parameters to produce expected changes are within the ability of one of ordinary skill in the part. Patentability over the prior art will only occur if the parameter variation produces an unexpected result. *In re Aller, Lacey and Hall*, 105 USPQ 233, 235. *In re Reese* 129 USPQ 402, 406.

11. With respect to claim 12, Yu does not disclose expressly wherein said offset of said LDD region from edges of said straight walled conductive gate structure is between about 50 to 100 Angstroms. However, Yu discloses the distance between LDD regions and the straight walled gate's edges can be adjusted by controlling various parameters (col. 11, lines 37-52). Any variation in distance between LDD regions and the straight walled gate's edges in the present claim is obvious in light of the cited art, because the

changes in distance between LDD regions and the straight walled gate's edges produce no unexpected function. The routine varying of parameters to produce expected changes are within the ability of one of ordinary skill in the part. Patentability over the prior art will only occur if the parameter variation produces an unexpected result. *In re Aller, Lacey and Hall*, 105 USPQ 233, 235. *In re Reese* 129 USPQ 402, 406.

12. With respect to claim 13, Yu discloses said sidewall spacers on said straight walled conductive gate structure are comprised of either silicon oxide or silicon nitride (col. 2, lines 21-26), but Yu does not disclose expressly wherein the sidewall spacers with thickness between about 200 to 800 Angstrom. However, any variation in sidewall spacers' thickness in the present claim is obvious in light of the cited art, because the changes in sidewall spacers' thickness produce no unexpected function. The routine varying of parameters to produce expected changes are within the ability of one of ordinary skill in the part. Patentability over the prior art will only occur if the parameter variation produces an unexpected result. *In re Aller, Lacey and Hall*, 105 USPQ 233, 235. *In re Reese* 129 USPQ 402, 406.

13. Claims 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu in view of Tabara (US Pat 5707883).

14. With respect to claim 4, Yu does not disclose expressly wherein said conductive layer is a doped polysilicon layer.

Tabara discloses a polysilicon conductive layer doped with n-type impurities (col. 4, lines 12-19).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the doped polysilicon conductive layer, as taught by Tabara.

The motivation for doing so would have been to lower its resistivity sufficient for use as a wiring or electrode (col. 4, lines 15-18).

15. With respect to claim 11, Yu discloses the anisotropic etching, but Yu does not disclose expressly wherein second etch procedure is a RIE procedure performed at a power between about 800 to 1000 watts, and at a pressure between about 50 to 100 mtorr, using Cl_2, HBr, O_2, and N_2 as etchants. Any variation in etching power and pressure in the present claim is obvious in light of the cited art, because the changes in etching power and pressure produce no unexpected function. The routine varying of parameters to produce expected changes are within the ability of one of ordinary skill in the part. Patentability over the prior art will only occur if the parameter variation produces an unexpected result. *In re Aller, Lacey and Hall*, 105 USPQ 233, 235. *In re Reese* 129 USPQ 402, 406.

Tabara discloses anisotropic dry etching process for polysilicon using using Cl_2, HBr, O_2, and N_2 as etching gas (col. 4, lines 51-55; col. 11, lines 1-13). Tabara also discloses an anisotropic reactive ion etching (RIE) to form sidewall spacers (col. 7, lines 25-41). So, the examiner takes the position that it is obvious to perform same RIE etching process for sidewall spacers to obtain shaped polysilicon.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the etching process to obtain the shaped polysilicon, as taught by Tabara.

The motivation for doing so would have been to achieve better control for etching process to obtain desired polysilicon shape.

16. Claims 15-17, 23-24, and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satoh et al. (US Pat 5834817; hereinafter "Satoh").

17. With respect to claim 15, referring to figures 5A-8C, Satoh discloses a method of forming a MOSFET device on a semiconductor substrate (col. 9, lines 49-55) featuring an LDD region offset from a portion of said semiconductor substrate located underlying the edges of a polysilicon gate structure (col. 8, line 63-col. 9, line 5), comprising the steps of: forming an gate insulator layer 2 on said semiconductor substrate 1; forming a polysilicon layer 3 on said gate insulator layer; forming a mask shape 11 on said polysilicon layer; performing a dry etch procedure (col. 5, lines 52-63) using said mask shape as an etch mask to define a polysilicon gate structure from said polysilicon layer, wherein said polysilicon gate structure is comprised with a top portion 3b featuring vertical sides, and comprised with a bottom portion 3a featuring notches or voids at polysilicon - gate insulator layer interface, with said notches in said bottom portion of said polysilicon gate structure exposing a first portion of said semiconductor substrate (see fig. 5E) while non-notched area of said bottom portion of said polysilicon gate structure is located overlying a second portion of said semiconductor substrate (figs. 6C, 6D, 8A); performing a first ion implantation procedure (col. 9, lines 6-14) to form said LDD region 4 in a third portion of said semiconductor substrate, wherein said third portion of said semiconductor substrate is not overlaid by said top portion of said

polysilicon gate structure (see fig. 8A); removing said mask shape (figs. 5D-5E); forming insulator spacers 5 on sides of said polysilicon gate structure filling said voids at said polysilicon - gate insulator layer interface; and performing a second ion implantation procedure (col. 9, lines 21-33) to form a heavily doped source/drain region 6 in a area of said semiconductor substrate not covered by said polysilicon gate structure or by said insulator spacers (see fig. 8C). Satoh discloses a mask shape, and anisotropic RIE etching process to form the shaped gate electrode (col. 10, lines 12-20; col. 5, lines 52-63), but Satoh does not disclose expressly performing a etch procedure to define the mask shape from mask layer. However, the examiner takes the position that it is obvious to perform similar etching process for the shaped gate electrode to obtain the mask shape.

18. With respect to claim 16, Satoh discloses said MOSFET device is an N channel (NMOS) device (col. 9, lines 49-55).

19. With respect to claim 17, Satoh discloses said MOSFET device is a P channel (PMOS) device (col. 9, lines 49-55).

20. With respect to claim 23, Satoh discloses said notches located in said bottom portion of said polysilicon gate structure, but Satoh does not disclose expressly wherein notches extend inwards between about 150 to 200 Angstroms from the vertical sides of said top portion of said polysilicon gate structure. However, any variation in notches' length in the present claim is obvious in light of the cited art, because the changes in notches' length produce no unexpected function. The routine varying of parameters to produce expected changes are within the ability of one of ordinary skill in the part.

Patentability over the prior art will only occur if the parameter variation produces an unexpected result. *In re Aller, Lacey and Hall*, 105 USPQ 233, 235. *In re Reese* 129 USPQ 402, 406.

21. With respect to claims 24 and 27, Satoh discloses wherein [Claim 24] said first ion implantation procedure used to form said LDD region, is performed at a dose between about 1E12 to 1E14 atoms/cm^2 (col. 9, lines 6-14), and at an implant angle of 0 degrees (see fig. 8A); [Claim 27] said second ion implantation procedure used to form said heavily doped source/drain region, but Satoh does not disclose expressly wherein the ion implantation procedure is performed using arsenic or phosphorous ions at an energy between about 3 to 10 KeV for LDD region, and between about 30 to 100 KeV and at a dose between about 1E15 to 1E16 atoms/cm^2 for heavily doped source/drain region. However, Satoh discloses phosphorous or arsenic ion impurities to implant into the polysilicon gate structure for etching rate purpose (col. 6, lines 6-26), so the examiner takes the position that it is obvious to use same ion impurities for polysilicon gate to form LDD region and heavily doped source/drain region. Satoh discloses a high concentration of more than $5x10^{14}/cm^2$ for heavily doped source/drain region (col. 9, lines 21-33). So, Satoh's dose concentration may overlap with claimed rages. In the case where claimed ranges "overlap or lie inside rages disclosed by the prior art" a prima facie case of obviousness exists. *In re Wertheim*, 541 F. 2d 257, 191 USPQ 90 (CCPA 1976); *In re Woodruff*, 919 F. 2d 1575, 16 USPQ 2d 1934 (Fed. Cir. 1990). Also, the arguments concerning ion implantation energy stated in claims 10 and 14 also apply.

22. With respect to claim 26, Satoh discloses said insulator spacers on sides of said polysilicon structure are comprised of either silicon oxide or silicon nitride (col. 9, lines 14-20), but Satoh does not disclose expressly the insulator spacers at a thickness between about 200 to 800 Angstroms. The arguments concerning sidewall spacers' thickness stated in claim 13 also apply.

23. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satoh in view of Quek (US Pub 2004/0157397).

24. With respect to claim 18, Satoh discloses the gate insulator layer, but Satoh does not disclose expressly wherein the gate insulator layer is obtained via thermal oxidation procedures to a thickness between about 10 to 80 Angstrom.

Quek discloses a gate insulator layer thermally grown in an oxygen-steam or in an oxygen ambient to a thickness between about 10 to 20 Angstroms. The arguments concerning overlapping range stated in claim 27 also apply.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to perform thermal oxidation to grow the gate insulator layer, as taught by Quek.

The motivation for doing so would have been to produce silicon oxide films with controlled thickness and silicon/silicon oxide interface properties.

25. With respect to claim 19, Satoh discloses said polysilicon layer is a doped polysilicon layer (col. 6, lines 6-26), but Satoh does not disclose expressly wherein said doped polysilicon layer is obtained via LPCVD procedures at a thickness between about

800 to 2000 Angstroms, and wherein said polysilicon layer is in situ doped during deposition via the addition of arsine or phosphine to a silane or to a disilane ambient.

Quek discloses a doped polysilicon layer can be obtained via LPCVD or PECVD procedures with the polysilicon layer in situ doped during deposition via the addition of arsine or phosphine to a silane or disilane ambient. And the thickness of the doped polyslicon layer is between about 1000 to 2500 Angstroms (page 2, paragraph 12). The arguments concerning overlapping range stated in claim 27 also apply.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to perform LPCVD procedure to form the doped polysilicon layer, as taught by Quek.

The motivation for doing so would have been to achieve precise control of composition and structure, low-temperature processing, and fast deposition rates.

26. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satoh in view of Tabara.

27. With respect to claim 20, Satoh discloses the mask layer, but Satoh does not disclose expressly wherein the mask layer is a silicon nitride layer obtained via LPCVD or via PECVD procedures at a thickness between about 200 to 800 Angstroms.

Tabara discloses a silicon nitride layer as an etching mask is formed via plasma CVD procedure (col. 5, lines 61-67), and the thickness of 50 to 60 nm (col. 5, lines 1-4). The arguments concerning overlapping range stated in claim 27 also apply.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use silicon nitride as a mask layer obtained via PECVD procedure, as taught by Tabara.

The motivation for doing so would have been to achieve formation of silicon nitride to protect against scratches at lower temperature.

28. With respect to claim 21, Satoh discloses said first dry etch procedure used to form said said mask shape is an anisotropic RIE procedure (see arguments stated in claim 15), but Satoh does not disclose expressly wherein the etching procedure is performed using either CF_4, C_4F_8, CHF_3 or CH_2F_2 as an etchant.

Tabara discloses an anisotropic dry etch to form patterned silicon nitride using CF_4 as the etching gas (col. 4, lines 39-45).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the etchant to obtain the shaped mask, as taught by Tabara.

The motivation for doing so would have been to achieve better control for etching process to obtain desired mask shape.

29. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Satoh in view of Liaw (US Pat 5807779).

Satoh discloses removing the mask shape, but Satoh does not disclose expressly wherein the mask shape is removed using a hot phosphoric acid solution.

Liaw discloses removing the masking pattern using hot phosphoric acid (col. 3, lines 36-41).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use hot phosphoric acid to remove the mask shape, as taught by Liaw.

The motivation for doing so would have been to use the conventional wet etching solution to remove the mask.

Allowable Subject Matter

30. Claims 8 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: claims 8 and 22 recite Cl_2, HBr, O_2, CF_4, N_2 and He as etchants for the ploysilicon layer, this feature in combination with the other elements of the claim is neither disclosed nor suggested by the prior art of record.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cheung Lee whose telephone number is 571-272-5977. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cheung Lee

October 17, 2005

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER